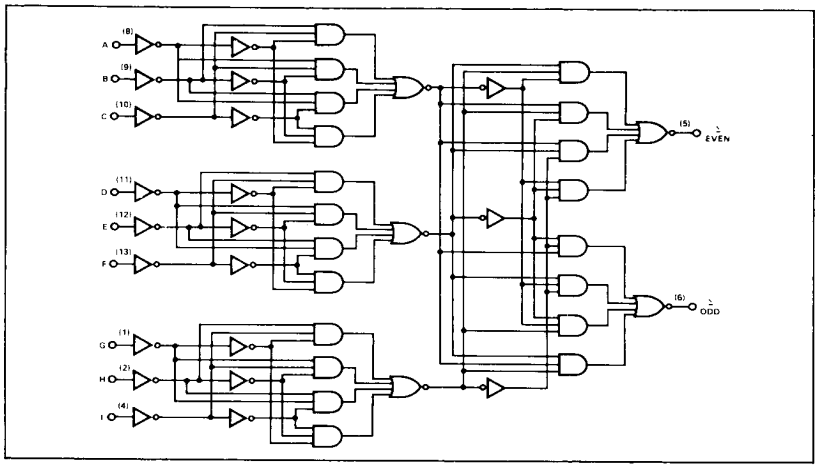
## BLOCK DIAGRAM






### SPEED/PACKAGE AVAILABILITY

54LS F,W 74LS B

### DESCRIPTION

This improved full adder performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. This adder features full internal look ahead across all four bits generating the carry term in ten nanoseconds typically. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

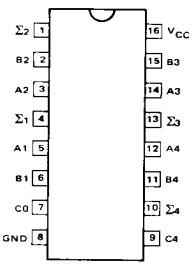
### SWITCHING CHARACTERISTICS $V_{CC}$ = 5V, $T_A$ = 25°C

| PARAMETER★ | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | LIMITS MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$<br>$t_{PHL}$ | C0 | Any Σ | $C_L$ = 15pF,<br>$R_L$ = 2kΩ | | 16<br>15 | 24<br>24 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | $A_i$ or $B_i$ | $\Sigma_i$ | | | 15<br>15 | 24<br>24 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | C0 | C4 | | | 11<br>11 | 17<br>17 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | $A_i$ or $B_i$ | C4 | | | 11<br>12 | 17<br>17 | ns |

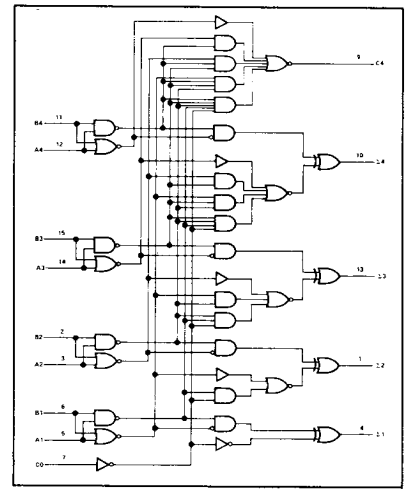
★$t_{PLH}$ = propagation delay time, low-to-high-level output
$t_{PHL}$ = propagation delay time, high-to-low-level output
Load circuit and waveforms are shown at the front of the book.

### PIN CONFIGURATION

B,F,W PACKAGE




### BLOCK DIAGRAM





signetics

### TRUTH TABLE

| INPUT | | | | OUTPUT | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | WHEN CO=L | | | WHEN CO=H | | |
| | | | | | | WHEN C2=L | | | WHEN C2=H |
| A1 | B1 | A2 | B2 | Σ1 | Σ2 | C2 | Σ1 | Σ2 | C2 |
| A3 | B3 | A4 | B4 | Σ3 | Σ4 | C4 | Σ3 | Σ4 | C4 |
| L | L | L | L | L | L | L | H | L | L |
| H | L | L | L | H | L | L | L | H | L |
| L | H | L | L | H | L | L | L | H | L |
| H | H | L | L | L | H | L | H | H | L |
| L | L | H | L | L | H | L | H | H | L |
| H | L | H | L | H | H | L | L | L | H |
| L | H | H | L | H | H | L | L | L | H |
| H | H | H | L | L | L | H | H | L | H |
| L | L | L | H | L | H | L | H | H | L |
| H | L | L | H | H | H | L | L | L | H |
| L | H | L | H | H | H | L | L | L | H |
| H | H | L | H | L | L | H | H | L | H |
| L | L | H | H | L | L | H | H | L | H |
| H | L | H | H | H | L | H | L | H | H |
| L | H | H | H | H | L | H | L | H | H |
| H | H | H | H | L | H | H | H | H | H |

H = high level, L = low level

NOTE: Input conditions at A1, B1, A, B2, and CO are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4, are then used to determine outputs Σ3, Σ4, and C4.

LOGIC

## DECADE COUNTER 54/74290

### SPEED/PACKAGE AVAILABILITY
54LS F,W 74LS A

### DESCRIPTION
This monolithic counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

The 54/74LS290 has a gated zero reset and has gated set-to-nine inputs for use in BCD nine's complement applications.

To use the maximum count length (decade or four-bit binary) of these counters, the B input is connected to the $Q_A$ output. The input count pulses are applied to input A and the outputs are as described in the function table. A symmetrical divide-by-ten count can be obtained by connecting the $Q_D$ output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output $Q_A$.

### PIN CONFIGURATION

A,F,W PACKAGE